In the Claims:

Claim 10 (amended). A method for manufacturing a memory cell array, which comprises:

applying a first insulating layer to a carrier wafer;

producing a trench having side walls and a bottom in the first insulating layer;

a1 producing a first yoke that adjoins the side walls of the trench and that adjoins the bottom of the trench, and producing the first yoke from a magnetizable material with a permeability of at least 10;

producing a first line in the trench;

producing a memory element with magnetoresistive effect above the first yoke and connecting the memory element to the first line;

producing a second line above the memory element and connecting the second line to the memory element;

insuring that the memory element is configured at a point of intersection between the first line and the second line;

B1 a

switching the memory element between the first line and the second line;

configuring the first yoke such that a magnetic flux through the first yoke is essentially closed in the memory element;

a1 cont.

during a write access, supplying current to a given line selected from a group consisting of the first line and the second line; and

partially surrounding the given line with the first yoke.

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a